Research Article

Three-dimensional Modeling of Core-structured Field Effect Transistor

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Abstract

Objective: In our previous publication, a core-structured field effect transistor (CoreFET) device shows field effect transistor (FET) behavior. In this work, we investigated factors such as the thickness of the film and the channel on the conductivity of the device in order to optimize the geometry to provide guidance on the fabrication of the device with the best performance.

Methods: This study uses Silvaco ATLAS numerical simulation software to investigate the performance of CoreFET. The effects of the thickness of the dielectric layer, \(\text{SiO}_2\), and the distance between the drain and source (channel length) on the conductivity of the semi-conductor indium gallium zinc oxide (IGZO) have been studied. The flat FET models with the same parameters were used for comparison.

Results: Our simulation results demonstrate a directed correlation between the optimized conductivity of the device and the thickness of the dielectric material, as well as the length of the channel. Enhanced sensitivity is achievable by employing a thinner dielectric layer and a narrower channel.

Conclusion: According to the results, the device can achieve better performance by optimizing the thickness of the insulator and the gap distance between drain and source electrodes. The remarkable similarity between them indicates that the FET effect remained largely unaffected by variations in FET shape. This observation suggests a consistent outcome across FETs, reinforcing the notion that CoreFET exhibits comparable results as those of film FETs. This finding significantly broadens the scope of CoreFET applications.

Keywords: transistor, FET, simulation

1 INTRODUCTION

Small and sensitive microsensors can be fabricated using the state-of-the-art micro/nano-electro-mechanical systems (MEMS and NEMS). Field-effect transistors (FETs) have found extensive applications in microelectronic devices, serving as the foundation for contemporary digital integrated circuits\textsuperscript{[1]} and even extending to applications like ignition coils in combustion engines\textsuperscript{[2]}. Diverse FET implementations have been explored\textsuperscript{[3-9]}. Among these, thin film transistors (TFTs) stand out as the most popular FET variants, typically
featuring a geometry with a bottom gate and a top drain/source.\cite{10-15} Despite their widespread use, the majority of existing FETs are manufactured using intricate and costly micromanufacturing processes. Furthermore, the challenge associated with these devices is the difficulty to be applied for detection of chemical and biological species inside a cell because the diameter of the devices — they are generally too big so it will damage the cell membrane. The adoption of a FET design that circumvents these complex processes can enhance accessibility for researchers in various fields.

Recently, we presented a groundbreaking proof-of-concept core field effect transistor (CoreFET) design based on a thin wire structure, which eliminates the need for micromanufacturing processes. The term “CoreFET” is coined to reflect the distinctive structure and design of the device. The novel wire shape and design make it particularly well-suited for various applications in flexible electronic and optoelectronic devices, including chemical and biological sensors. In this innovative device, the core of a metal wire serves as the gate terminal, covered with a thin film of dielectric material — either SiO\(_2\) or polyethylene glycol terephthalate (PGT) in our experiments. A semiconductive material film is then applied to the dielectric materials, and this semiconductor body is linked to the source (S) and drain (D) terminals. This design proves advantageous for specific applications, such as chemical field-effect transistor sensing. The exposed semiconductive sensing material interacts with the external environment, enabling the detection of chemicals, especially in small volumes like living cells, thanks to the unique thin wire design.

It is anticipated that this CoreFET sensing device will be used for sensing the same way as a regular FET, but can be used for specialty applications, such as for the in vivo test.

In our previous publication, the CoreFET device shows FET behavior when the semiconductor materials are n-type ZnO and p-type poly(3-hexylthiophene) (P3HT)\cite{16}. However, the results from our device show low on/off ratios. In this work, we investigated factors such as the thickness of the film and the channel on the conductivity of the device in order to optimize the geometry to provide guidance on the fabrication of the device with the best performance. Indium gallium zinc oxide (IGZO) has attracted attention due to its great performance\cite{17}, so we simulated the device based on IGZO and the results are compared with those using a traditional flat FET sensing design\cite{18}.

2 MATERIALS AND METHODS
2.1 Numerical Simulation

The term technology computer-aided design (TCAD) generally encompasses a suite of software tools that facilitate semiconductor process simulation and device simulation. It has been used in the semiconductor industry to simulate the semiconductor fabrication process and predict the electrical behavior of fabricated devices\cite{19}. The semiconductor industry is becoming more reliant on TCAD tools as technology continues to evolve and become more complex. The use of TCAD has become essential to reduce costs and improve the efficiency of research and development processes. TCAD typically simulates individual devices, and sometimes can be used for multiple devices. For a process simulator, the typical fabrication process steps (diffusion, oxidation, deposition, etching, ion implantation, and annealing) must be considered\cite{20}. Device simulators solve fundamental, physical, and partial differential equations.

Silvaco covers a wide range of fields in the semiconductor industry, among which ATLAS is one of the world’s most popular commercial TCAD tools. ATLAS is a powerful device simulation system that can simulate the electrical, optical, and thermal behavior of various semiconductor devices. This physics-based platform is easy to use and modular, allowing for flexible expansion to analyze the DC, AC, and time-domain responses of devices in 2D and 3D modes.

Computer simulation is based on numerical calculations. The numerical calculation in ATLAS is based on a series of physical models and equations. These equations are based on either mature solid-state physics and semiconductor physics theories or some empirical formulas. ATLAS provides a flexible way to set the quantity of the equation. They can be set to a fixed value, such as \( \mu = 1.200 \text{cm}^2/\text{V} \cdot \text{s} \), or can be described by a custom function. This requires a C interpreter to write the corresponding function expression file. If the corresponding physical model describes the parameters, the parameters are calculated from other model equations.

In ATLAS, the simulation area is divided into grids, and the desired characteristics, such as electrical properties and optical properties, are calculated at the grid points. Grid division is important for simulation. A finer grid can result in more accurate results, but it will increase the calculation time accordingly and may also cause non-convergence. Therefore, grid points are important resources for calculations and should be used reasonably.

The accuracy of the simulation is related to the physical model selected. Physics-based calculation means that the equations used in the simulation calculation have physical meaning, and different physical models are used in different applications. ATLAS simulation models are based on mature results, which are usually published in IEEE. Silvaco adopted these results and created the Silvaco library.

In the actual situation, the characteristics of the device must be tested using instruments. The test result is usually the terminal current and voltage characteristics, which can be changed with ambient temperature, light, pressure, or magnetic field, etc. ATLAS also follows this idea when
performing device simulation. In addition to obtaining the electrical characteristics of the terminal, ATLAS can also obtain the internal information of the device, like concentration distribution, potential distribution, current density, etc., which is difficult for actual test equipment.

ATLAS can input material parameters, such as mobility parameters, energy band parameters, dielectric constants, etc., and can change the parameter values of the physical model. As for semiconductors, the parameters include electron affinity, band gap, density of state, saturation rate, etc.

The density of states (DOS) model is used in the FET simulation. ATLAS treats the DOS \( g(E) \) as four parameterized components (Equation 1): two tail bands, the acceptor-like exponential \( g_{TA} \) and the donor-like exponential function \( g_{TD} \) and two deep level bands modeling using a Gaussian distribution, the acceptor-like Gaussian function \( g_{GA} \), and the donor-like Gaussian function \( g_{GD} \).[21]

\[
g(E) = g_{TA}(E) + g_{TD}(E) + g_{GA}(E) + g_{GD}(E) \tag{1}
\]

\[
g_{TA}(E) = N_{TA} \exp \left[ -\frac{E - E_c}{W_{TA}} \right] \tag{2}
\]

\[
g_{TD}(E) = N_{TD} \exp \left[ -\frac{E - E_v}{W_{TD}} \right] \tag{3}
\]

\[
g_{GA}(E) = N_{GA} \exp \left[ -\frac{(E_{GA} - E)^2}{W_{GA}} \right] \tag{4}
\]

\[
g_{GD}(E) = N_{GD} \exp \left[ -\frac{(E - E_{GD})^2}{W_{GD}} \right] \tag{5}
\]

In the equations, \( E \) is the trap energy, \( E_c \) is the conduction band energy and \( E_v \) is the valence band energy. As for the subscripts, \( T \) stands for tail, \( G \) represents Gaussian, \( A \) and \( D \) are acceptor and donor states, respectively.

Equations 2 and 3 describe the DOSs, \( g_{TA} \) and \( g_{TD} \), respectively, in an exponential tail distribution. These equations incorporate \( N_{TA} \) and \( N_{TD} \) which denote the intercept densities at the conduction and valence band edges, and \( W_{TA} \) and \( W_{TD} \) which represent the characteristic decay energies.

As for Gaussian distribution, the DOSs \( g_{GA} \) and \( g_{GD} \) are described by Equations 4 and 5, in which \( N_{GA} \) and \( N_{GD} \) are the intercept densities, \( W_{GA} \) and \( W_{GD} \) are the characteristic decay energies and \( E_{GA} \) and \( E_{GD} \) are the peak energies.

2.2 Experiment

Based on the schematic design shown in Figure 1, a 3D model of the devices was constructed. Given that a-IGZO is classified as an n-type semiconductor and a-IGZO TFTs operate primarily in the n-channel mode, it is essential to consider the acceptor-like states, specifically \( g_{TA} \) and \( g_{GA} \). The simulation parameters of a-IGZO are consistent with the model introduced by Fung’s group.[18] Illustrated in Figure 2 is a flat FET model employed for comparison. The device parameters for the CoreFET are the same as those in a thin film flat FET used for reference. The thickness of the dielectric layer, SiO\(_2\), is 100nm, the length of the channel is 6\( \mu \)m, and the thickness of the active layer (IGZO) is 20nm. It is noteworthy that to keep all the parameters in the CoreFET model the same as those in the thin film flat FET model, the shape of the wire should be considered for accurate calculation. For instance, the width of the channel...
changes when the thickness of the dielectric layer changes on the wire (The wire perimeter within the CoreFET is identical to the channel width in the traditional film FET, See Figures 1 and 2 for the illustration). Thus, we used the average width of the channel of various thicknesses. Table 1 shows the relationship between the width of the channel and the thickness of the dielectric layer calculated according to the following equation:

\[
\text{Width of the channel} = \text{perimeter of the (wire + } \frac{1}{2} \text{ thickness of the film)} = 2\pi r (r = \text{wire radius + } \frac{1}{2} \text{ thickness of the film}), \text{ the wire radius} = 2.5\mu m.
\]

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<th>Thickness (nm)</th>
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3 RESULTS AND DISCUSSION

3.1 The I-V Characteristics of CoreFET and Flat Thin Film FET

The I-V curves of the thin film flat FET and the CoreFET were simulated using ATLAS. The I-V curves of the thin film flat FET were simulated to provide a baseline for comparison. This comparison serves to assess the performance of the CoreFET as against that of a conventional thin film flat FET device. The simulated I-V characteristics of thin film flat FET (Figure 3A) matched the results reported in a reference paper[10]. Notably, the CoreFET device exhibits remarkably similar profiles (Figure 3B), mirroring its thin film flat FET counterpart. In both simulated devices, the current increased and gradually reached a plateau when the gate voltage increased from 0 to 20V, indicating a typical transistor character. The on/off ratio for the device is over $10^{10}$.

3.2 Effect of the Thickness of the Insulator on the Conductivity

Figure 4A shows that a decrease in the thickness of the insulator (dielectric) caused an increase in the source-drain current. When the thickness decreased from 2µm to 30nm, the current underwent a substantial increase from $1.0 \times 10^{-7}$A to $7.5 \times 10^{-6}$A at the 20V gate voltage, making a 75-fold increase in the current. It is also noteworthy that, when the thickness of the insulator decreased from 2µm to 1µm, there is minimal impact on the current. However, a more pronounced increase in current was observed when the thickness decreased from 50nm to 30nm. This relationship between the thickness of the insulator and the performance of the device was also observed from Ding’s group[12]. The enhanced performance with a thinner insulator is attributed to its larger capacitance. The influence of insulator thickness on the CoreFET device’s conductivity mirrors that observed in the thin film flat FET device (Figure 4B).

As depicted in Figure 5, the current plotted against thickness and the current intensity for both devices exhibit striking similarity. This outcome underscores the significant impact of the insulator thickness on the electric characteristics output of the CoreFET device. To enhance the performance of CoreFET, it is evident that reducing the thickness of the insulator layer is a promising avenue for future improvements.

3.3 The Effect of the Gap Distance Between the Source and Drain on the Conductivity

The simulation result shows that a decrease in the gap between the source and drain electrodes caused an increase in the source-drain current. Figure 6A shows that when the gap decreased from 8µm to 1µm, the current changes from $1.5 \times 10^{-6}$A to $1 \times 10^{-5}$A at a 20V gate voltage, approximately a 6-fold increase in the current intensity.
Figure 4. The drain current vs gate voltage of a CoreFET device (A) and a thin film flat FET device (B), when the drain voltage was 0.1V. The thickness of the dielectric material of the device was 30nm, 50nm, 100nm, 200nm, 300nm, 500nm, 1μm, and 2μm.

Figure 5. The comparison of the drain current vs. the dielectric thickness of the CoreFET device and the thin film flat FET device, when the gate voltage is 5V and the drain voltage is 0.1V for different dielectric thickness.

The conductivity is approximately inversely proportional to the gap distance between the electrodes. The effect of the gap between the two electrodes on the conductivity of the CoreFET device is similar to that of a thin film flat FET device (Figure 6B).

Figure 6. The source-drain current vs. the gate voltage of a CoreFET device (A) and a thin film flat FET device (B), when the drain voltage is 0.1V. The distance between the drain and source (channel length) is 1μm, 2μm, 3μm, 4μm, 5μm, 6μm, 7μm, and 8μm. The thickness of the SiO$_2$ is 100nm.

Figure 7 shows that the current vs gap profiles of the two devices are very close to each other.

4 CONCLUSION

The electrical characteristics of a CoreFET were investigated alongside a thin film flat FET using Silvaco ATLAS. Upon comparing the simulation outcomes with the results from a previous experiment, a notable distinction emerges, primarily in the on/off ratio of the devices. The simulated devices exhibit an on/off ratio surpassing $10^{10}$, with a more pronounced saturation mode compared to the experimental results.

Based on the simulation results for CoreFET and thin film flat FET, it is evident that the performance of CoreFET is on par with that of a thin film flat FET. This implies that the lower performance observed in the experimental results is not attributed to the device design but rather to the fabrication quality. Key factors influencing FET performance encompass the thickness of the dielectric layer, channel length, device configuration (including electrode contacts), thickness of the active layer, and the dielectric material. In this study, we specifically investigated the impact of the dielectric material thickness and the gap between the source and drain
The thickness of the SiO₂ is 100nm.

electrodes on the current. The findings reveal that the current increases with a decrease in dielectric layer thickness or channel length. Consequently, optimizing the thickness of the insulator and the gap distance between the drain and source electrodes can lead to improved device performance.

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Conflicts of Interest
The authors declared no conflict of interest.

Author Contribution
Chen K was responsible for data curation and original draft preparation. Ji HF was responsible for review, editing and supervision. The authors have read and agreed to the published version of the manuscript.

Abbreviation List
CoreFET, Core field effect transistor
DOS, Density of states
FET, Field effect transistor
IGZO, Indium gallium zinc oxide
TCAD, Technology computer-aided design
TFTs, Thin film transistors

References

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Figure 7. The comparison of the source-drain current of a CoreFET device and a thin film flat FET device, when the gate voltage is 5V and the drain voltage is 0.1V for different channel lengths.